REMARKS

The Examiner rejected claims 2-7, 9 and 11-21 under 35 U.S.C. 102 (b) as being unpatentable over Guddat et al. (U.S. Patent 6,366,990).

Applicants contend the Examiners rejection of claims 11 and 21 is moot in light of Applicants cancellation of claims 11 and 21.

Applicants respectfully traverse the §102(b) rejections with the following arguments.

As to claims 2-6 and 12-20 , the Examiner states that "Guddat et al. disclose an electronic circuit (Figure 1), a memory cell array (106); a sense amplifier self-timed decode circuit (172,116,139) adapted to set a base read time delay of the memory cell array (Column 8, lines 53-65, Column 9, lines 1629, Column); a read delay adjustment circuit (Column 3, lines 40-61, Column 9, lines 2950) coupled to the memory cell array, the read delay adjustment circuit adapted to adjust the based read time delay of the memory cell array based on an operating frequency of the memory cell array; a sense amplifier delay circuit (139,151) Column coupled between the sense amplifier self-timed decode circuit and the memory cell array, the sense amplifier delay circuit adapted to the control an amount of the delay time added to the base read time delay in response to a margin select signal (Column 29-67, Column 10, lines 1-60); and a read margin adjustment circuit (Column 9, lines 37-67, Column 10, lines 1-8) coupled to the sense amplifier delay circuit, the read margin adjustment circuit adapted to generate the margin select signal, and a microprocessor (Column I , lines 11- 40, Column 3, lines 12-32) adapted to execute a load instruction issued in response to a change of value of the operating frequency of the microprocessor and of the memory cell array and to store data associated with the load instruction in a register, an output of the register coupled to the sense amplifier delay circuit (Column 4, lines 14-48), and wherein the read margin circuit includes a frequency selection circuit adapted the operating frequency of the memory cell array from internal generation circuit or from external clock signal, and frequency detector coupled between the frequency selection circuit and the sense amplifier delay circuit (Column 3, lines 40_55), and including one or more programmable fuses (Figure 1, 139) coupled to the sense amplifier delay circuit, the sense amplifier adapted to set an initial time adjustment to the base read time delay based on a state of one or more fuses (Column 3, lines 55-67, Column 4, lines 1-

22), and the sense amplifier delay circuit is adapted to override the initial time adjustment based on the margin select signal (Column 4, lines 14-22), and when the operating frequency is to be decreased, sequentially decreasing the operating frequency, issuing the margin select signal and decreasing the operating voltage in the order recited and when the operating frequency is to be increased sequentially increasing the operating voltage , issuing the margin select signal and increasing the operating voltage in the order recited (Column 11, lines 18-48)."

Applicants contend that claim 2, as amended, is not anticipated by Guddet et al. because Guddet et al does not teach each and every feature of claim 2. In a first example, Guddet et al does not teach "said read margin adjustment circuit responsive to an operating frequency of said electronic device" Applicants respectfully point out Guddet et al. is does teach "programmable delay circuitry to alter the timing of I/O signals" but the programmable delay circuitry is not "responsive to an operating frequency" as Applicants claim 2 requires. Further, Applicants are unable to find the word "frequency" does not appear anywhere in Guddet et al. In fact, Guddet et al. specifically teaches in col. 1, lines 60-61 and col. 13 lines 49-43-45 that timing is controlled by software and in col. 5, lines 17-25 and FIG. 1, that the software responds to data representing user inputs from a patch logic interface 180.

In a second example, Guddet et al does not teach "a read margin adjustment circuit, said read margin circuit coupled to said sense amplifier delay circuit." The Examiner has indicated Guddet elements 172, 116 and 139 correspond to Applicants "sense amplifier self-timed decode circuit" and Guddet et al. elements 139 and 151 corresponding to Applicants "sense amplifier delay circuit" but has not identified any element of Guddetr et al. corresponding to "a read margin adjustment circuit." Further, the Examiner has identified Gudett et al. element 139 as

belonging to both Applicants "sense amplifier self-timed decode circuit" and Applicants "sense amplifier delay circuit" which is not possible.

Based on the preceding arguments, Applicants respectfully maintain that claim 2 is not unpatentable over Guddet et al and is in condition for allowance. Since claims 3-6 depend from claim 2, Applicants respectfully maintain that claims 3-6 are likewise in condition for allowance.

Applicants contend that claim 12 is not anticipated by Guddet et al. because Guddet et al does not teach each and every feature of claim 123. In a first example, Guddet et al does not teach "adjusting said base read time delay of said self-timed memory array based on an operating frequency of said electronic device." Applicants respectfully point out Guddet et al. does teach "programmable delay circuitry to alter the timing of I/O signals" but the programmable delay circuitry does not adjust "said base read time delay of said self-timed memory array based on an operating frequency of said electronic device" as Applicants claim 12 requires. Further, Applicants are unable to find the word "frequency" does not appear anywhere in Guddet et al. In fact, Guddet et al. specifically teaches in col. 1, lines 60-61 and col. 13 lines 49-43-45 that timing is controlled by software and in col. 5, lines 17-25 and FIG. 1, that the software responds to data representing user inputs from a patch logic interface 180.

In a second example, Guddet et al does not teach "a read margin adjustment circuit...said read margin circuit coupled to said sense amplifier delay circuit." The Examiner has indicated Guddet elements 172, 116 and 139 correspond to Applicants "sense amplifier self-timed decode circuit" and Guddet et al. elements 139 and 151 corresponding to Applicants "sense amplifier delay circuit" but has not identified any element of Guddetr et al. corresponding to "a read margin adjustment circuit." Further, the Examiner has identified Gudett et al. element 139 as

belonging to both Applicants "sense amplifier self-timed decode circuit" and Applicants "sense amplifier delay circuit" which is not possible.

Based on the preceding arguments, Applicants respectfully maintain that claim 12 is not unpatentable over Guddet et al and is in condition for allowance. Since claims 13-20 depend from claim 12, Applicants respectfully maintain that claims 13-20 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Canada et al.

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